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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,461	11/12/2003	Jae-Goo Lee	SAM-0270DIV	6750

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EXAMINER	
INGHAM, JOHN C	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/706,461	LEE, JAE-GOO	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. An English translation of applicant's foreign priority papers has been entered of record.

Response to Amendment

2. Applicant's amendment dated November 14th, 2005 in which the specification and claims 1-2 were amended has been entered of record.

Drawings

3. Previous objections to the drawings have been withdrawn based on Applicant's amendment.

Specification

4. Previous objections to the specification have been withdrawn based on Applicant's amendment.

Claim Objections

5. Previous objections to claim 1 have been withdrawn.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims **1, 2, 4, and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figures in view of Chang et al. (US 6,358,864), hereafter "Chang" ('864).

Regarding claim **1**, the applicant's prior art Figure 8 shows a semiconductor substrate (10) having a multi-layered spacer, comprising: a plurality of gate electrodes each including a gate oxide layer (15), a gate conductive layer (16), and a capping dielectric layer (17) formed on the semiconductor substrate; a gate polyoxide layer (19a) formed on sidewalls of the gate oxide layer and the gate conductive layer and being in contact with a portion of the semiconductor substrate, an oxide layer (20b) and an isotropically etched (page 2 lines 12-14) external spacer (22a) being in contact with an outer surface of the oxide layer.

The prior art also discloses in Figure 8 a portion of the semiconductor substrate exposed (14) between neighboring gate electrodes, wherein the outer ends of the gate polyoxide layer, the oxide layer, and a lower outer end of the external spacers are aligned. The claim language "exposed between neighboring gate electrodes by etching the oxide layer... using the external spacers and the gate electrode as an etch mask..."

describes a product by process. Products by process claims are not limited to the manipulations of the recited steps, only the resulting structure.

The prior art also discloses in Figure 8 a conductive pad (28) in a region between adjacent gate electrodes having the multi-layered spacer and being in contact with the exposed semiconductor substrate (10) and the external spacer (22a).

The prior art does not disclose a silicon nitride layer being in contact with the sidewalls of the capping dielectric layer and in contact with the gate polyoxide layer, nor does it disclose the oxide layer (20b) being in contact with the silicon nitride layer. The end result of the prior art is a sidewall spacer with an oxide/oxide/nitride (OON) structure.

Chang ('864) teaches a method of fabricating an oxide/nitride/oxide/nitride (ONON) multilayer structure. In column 4, on lines 18-21, Chang ('864) discloses that his method could be applied at the process of forming a multilayer spacer, such as an ONON.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the prior art with the method taught by Chang ('864) to arrive at a multilayered-spacer semiconductor structure, simply by inserting a nitride layer between the existing oxide layers. Motivation to do so would include the enhancement of the resistivity strength of the dielectric film (col. 1, ln. 20). Such a combination would result in ONON sidewall spacers on a plurality of gate electrodes, with conductive pads contacting the exposed substrate therebetween.

Regarding claim **2**, Applicant's prior art in Figure 8 discloses the semiconductor substrate of claim 1, further comprising an interlevel dielectric layer (30) formed on the pad and each gate electrode having the multi-layer spacer.

Regarding claim **4**, the claim language "wherein the gate polyoxide layer is an oxide layer formed at a temperature of about 800~900°C with the injection of oxygen" describes a product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Chang ('864) discloses an oxide layer formed at a temperature of 750-850°C with the injection of N_2O.

Regarding claim **6**, the claim language "wherein the oxide layer is an oxide layer formed at a temperature of about 600~800°C using $SiCl_4$ and O_2" describes a product-by-process. Chang ('864) discloses an oxide film formed by LPCVD at a temperature of 750-850°C using N_2O and SiH_2Cl_2, however, product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps. Therefore the structure of the instant oxide layer is not distinct from that of the disclosed oxide layer.

Regarding claim **7**, Chang ('864) teaches the claimed oxide layer. The claim language "wherein the oxide layer is a middle temperature oxide layer or a high temperature oxide layer having a dielectric constant of 3.9..." describes a product-by-process. Product-by-process claims are not limited to the manipulations of the recited steps, only the structure resultant from the steps; therefore the instant structure is not distinct from the structure disclosed by Chang ('864).

With regard to the thickness of the oxide layer, "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). See also the case of *In re Huang*, 40 USPQ2d 1685 (Fed. Cir. 1996), in particular the passage "Accordingly, one of ordinary skill would have experimented with various thicknesses to obtain an optimum range."

Regarding claim **8**, Chang ('864) discloses that the external spacer is formed of silicon nitride (col. 4, ln. 18-20).

9. Claims **3 and 5** are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's prior art figures in view of Chang ('864) as applied to claim 1 above, and further in view of Chang (US 5,817,562), hereinafter Chang ('562).

Regarding claim **3**, the applicant's prior art in view of Chang ('864) discloses the semiconductor substrate of claim 1, but does not disclose wherein the gate polyoxide layer prevents the silicon nitride layer from separating from the semiconductor substrate and has a thickness of about 50~100Å.

Chang ('562) discloses in Figure 5 a gate polyoxide layer (24) with a thickness of about 50~100Å (col 6 ln 15-16). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the structure of the applicant's prior art in view of Chang ('864), with the method used by Chang ('562) to form vertical gate electrodes with sidewall spacers. One would have been motivated to do so by the disclosure by Chang ('562) that contacts on the FET would be more reliable (col 1 ln

12). The claim language "wherein the gate polyoxide layer prevents the silicon nitride layer from separating from the semiconductor substrate" is functional language and not distinguishable over the prior art, because the polyoxide of Chang ('562) can perform the recited function.

Regarding claim **5**, Chang ('562) discloses that the silicon nitride layer ha a thickness of about 100-500Å (col 6 ln 26-30).

Response to Arguments

10. Applicant's arguments, see pages 6 and 7, filed 11/14/2005, with respect to claims 1, 2, 4, 6, and 8 as anticipated by Divakaruni, and claims 1, 4, and 6 as anticipated by Takahashi have been fully considered and are persuasive. The translated foreign priority papers have been made of record.

11. Applicant's arguments filed 11/14/2005 (see page 10) have been fully considered but they are not persuasive. In response to applicant's argument that Chang '864 is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, AAPA and Chang '864 are considered as analogous art since they are classified in solid-state devices and manufacturing. Chang '864 discloses a method for fabricating an oxide/nitride multilayer structure that *could* be

applied for manufacturing EPROM, flash memory, etc. However, as stated in column 4, lines 18-20, the method could also be applied at the process of forming a multilayer spacer.

12. In response to applicant's argument that the combined teachings of AAPA and Chang '864 do not suggest "a portion of the semiconductor substrate exposed between neighboring gate electrodes by etching the oxide layer, silicon nitride layer and gate polyoxide layer using the external spacers and the gate electrodes as an etch mask so that outer ends of the gate polyoxide layer, the silicon nitride layer, and the oxide layer, and a lower end of the external spacer are aligned", the structure as claimed is taught by the combination of AAPA and Chang '864. The claim language "exposed between neighboring gate electrodes by etching the oxide layer... using the external spacers and the gate electrode as an etch mask..." describes a product by process. Products by process claims are not limited to the manipulations of the recited steps, only the resulting structure. The argument that the silicon nitride layer can be used as an etch stop layer during the self-aligned etching process, and further as a blocking layer, describes the intended use of the invention and not a novel structure. Since the combination of AAPA and Chang '864 does teach the claimed structure, this argument is also non-persuasive.

Conclusion

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jci

GEORGE ECKERT
PRIMARY EXAMINER